McGill University
Department of Electrical and Computer Engineering

ECSE 324 Mid-Term Exam Fall 2020

Name: _____

ID:

Open Book Exam.

Part 1_____/10

Part 2 _____/10

Part 3 _____/6

Important information, please read it in full

Communication embargo: Please note that you are not allowed to communicate (online or offline) with anyone else about the content of this exam **until the end of the exam** (48h after the start time). If anyone tries to get in touch with you during this period to discuss the content of this exam, please report it immediately by email to the instructor (chrisotphe.dubach@mcgill.ca).

Response format: This PDF version is provided as a backup and should only be used in case you encounter issues with the online quiz on mycourses. If you decide to use this PDF for your exam, please return all your answers in a text file or PDF before the end of the exam. Each answer should be correctly labelled with the proper number from the corresponding question in the PDF. For answers requiring to fill in a table, simply use colons to separate the columns and a new line to separate the rows. For instance,

1	2	3
4	5	6

is written as:

1, 2, 3
4, 5, 6

Filename: The filename should be exactly:

McGillid_Firstname_Lastname.txt

where you replace Firstname, Lastname and McGillid with your specific information.

Email content: The text file should be sent by email as an **attachment** to the instructor (christophe.dubach@mcgill.ca) with an explanation as to why it is not possible for you to complete the quiz on mycourses. Please note that if you do send your responses by email, we will not look at any answers you may have entered on the online quiz.

In addition, please make sure to read and copy/paste the following text into your email.

By submitting this work, I certify that the work represents solely my own efforts. I confirm that I understand the meaning and consequences of cheating, plagiarism and other academic offences under the Code of Student Conduct and Disciplinary Procedures*, and am aware of my responsibilities under the* Student Assessment Policy*.*

A) General knowledge **[10 points]**

Short questions, **[1 point]** each. If more than answer is selected, you will get zero for that question.

1. Given a byte-addressable memory and a 12-bit address space, the maximum capacity of the memory is:

a)	b)	c)	d)	e)
12MB	4KB	8KB	4MB	None of These

2. The binary representation of the number 7 in 2's complement is:

a)	b)	c)	d)	e)
1010	1011	0101	1001	None of These

3. Which instruction(s) modify the ARM CPSR (Current program Status Register)?

a)	b)	c)	d)	e)
SUBS	TST	CMP	All of these	None of These

4. The ARM BL instruction:

a)	b)	c)	d)	e)
Modifies the Link Register	Modifies the Stack Pointer	Modifies the Program Counter	All of these	None of These

5. The Linker:

a)	b)	c)	d)	e)
Generates the Symbol Table	Generate the list of External References	Load the program into memory	All of these	None of These

6. Memory mapped I/O registers:

a)	b)	c)	d)	e)
Are physically in the main memory	Can be read by the processor with an LDR instruction	Are ready-only	All of these	None of These

7. Just before returning from a normal ARM interrupt service routine to a standard subroutine:

a)	b)	c)	d)	e)
the link register must be restored explicitly	the stack pointer must be restored explicitly	The CPSR must be restored explicitly	All of these	None of These

8. Bus arbitration is required when:

a)	b)	c)	d)	e)
more than one device may act as the bus master	several devices are connected to the same bus	using a parallel bus	all of these	none of These

9. Serial links are better than parallel links over longer distances because:

a)	b)	c)	d)	e)
the clock frequency can be higher	they don’t suffer from bus skew	an arbiter is not required	information travel faster on the wire	none of These

10. A PCI bus:

a)	b)	c)	d)	e)
is asynchronous	uses the same lanes for addresses and data	uses serial links	All of These	None of These

B) Problem analysis: ISA/Assembly **[10 points]**

Assume a 16-bits RISC CPU with 8 general purpose registers which includes a PC (Program Counter) register (R7), and a separate CPSR (Current Program Status Register). Assume that the memory is byte-addressable and that the only instructions available in the instruction set are:

- ADD Rd, Rs1, Rs2 // Rd <- Rs1 + Rs2
- SUB Rd, Rs1, Rs2 // Rd <- Rs1 - Rs2
- LD Rd, Rs1, Rs2 // Rd <- MEM[Rs1+Rs2]
- ST Rd, Rs1, Rs2 // MEM[Rs1+Rs2] <- Rd
- MOV Rd, #imm // Rd <- #imm (immediate value)

Also, assume that each instruction can be conditionally executed with one of the four conditions:

- EQ (equal)
  LE (less or equal)
  LT (less than)
  AL (always)

and assume that each instruction can update the CPSR when used with an S flag.

[6 points]

11. Design a binary encoding for this instruction set so that each instruction fits within 16-bit and **so as to maximize the maximum immediate value that can be represented.** Show which parts of the 16-bit instruction are used for opcode, conditions, S flag, registers, and/or immediate value.

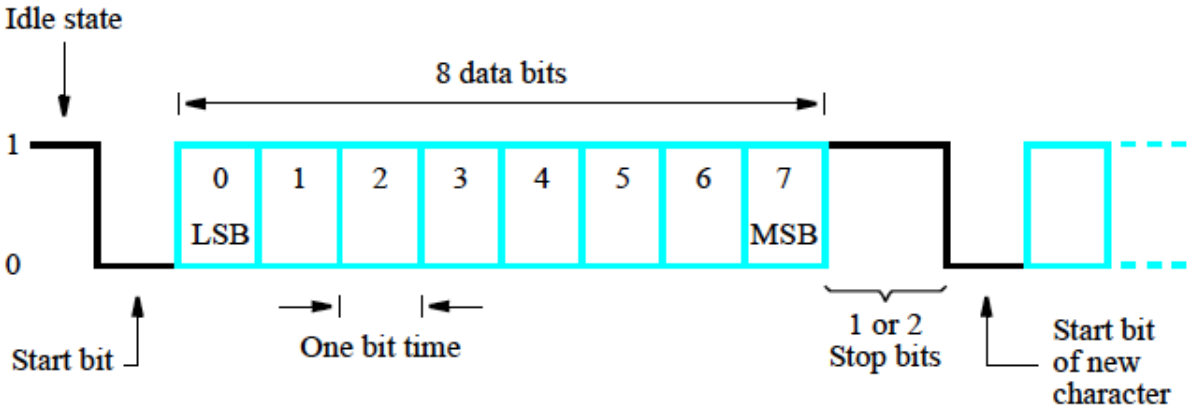
Show as well the encoding chosen for each opcode (ADD,SUB,LD,ST,MOV), condition (EQ,LE,LT,AL), S flag and register (R0, R1, ..., R7) (e.g. for ARM 32-bit, the GE condition code is encoded with 4 bits as “1010”).

[4 points]

12. The instruction set above does not have a branch nor a CMP instruction. Implement the following two pseudo-instructions using only the instructions above:

- CMP Rs1, Rs2 // update the CPSR based on the result of Rs1-Rs2
- BEQ #addr_offset // branch if condition is EQ, where addr_offset is an
  // immediate value corresponding to an address relative
  // to the current value of the PC

B) Problem analysis: UART **[6 points]**



As seen in the lecture, using a "start-top" scheme with the Universal Asynchronous Receiver Transmitter (UART) requires the receiver's clock to run at *approximately* 16x the speed of the transmitter clock to transfer 8 bits of information correctly.

We now transmit the following 8 bits, **10101010**, using the scheme above, which starts from the most-significant bit (a normally functioning receiving should receive the same digits in the same order, with the most significant digit being sent first).

[2 points]

13. Let's assume that the receiver clock runs at exactly 15.9x the speed of the transmitter. What will be the first 8 bits of data recognized by the receiver (before reaching the stop bit)?

[2 points]

14. Now, let's assume that the receiver clock is not so well calibrated and actually runs at exactly 18x the speed of the transmitter. What will be the first 8 bits of data recognized by the receiver (before reaching the stop bit)? Hint: in case the receiver clocks' edge at the count of 16 matches the transmitter clock's edge, pick either the bit value before or after.

[2 points]

15. Explain, **in your own word** and in 2-3 sentences, why the stop bits are required before the start bit.